## CLAIMS

What is claimed is:

1. A computer system, comprising:

a CPU;

a memory controller coupled to said CPU;

a system memory coupled to said memory controller, with said memory controller controlling and formatting transactions to the system memory;

wherein said memory controller runs calibration cycles to said system memory to re-calibrate said system memory, and wherein said memory controller is capable of varying the frequency of said calibration cycles based on at least one parameter that may affect the operation of the system memory.

2. The system of claim 1, further comprising an environmental sensor that couples to said memory controller to provide a signal to said memory controller representing at least one environmental parameter, and wherein said memory controller is capable of changing the frequency of the calibration cycles in response to the signal from said environmental sensor.

3. The system of claim 2, wherein the calibration cycles comprise a temperature calibration cycle.

4. The system of claim 2, wherein the calibration cycles comprise a current calibration cycle.

5. The system of claim 2, wherein said environmental sensor comprises at least one temperature sensor.

6. The system of claim 5, wherein the system memory comprises a plurality of RDRAM devices, and wherein said temperature sensor is located adjacent said RDRAM devices.

7. The system of claim 6, further comprising a second environmental sensor located adjacent said RDRAM devices to measure a second environmental parameter.

8. The system of claim 7, wherein the second environmental sensor measures humidity in the vicinity of the RDRAM devices, and provides a signal indicating humidity in the vicinity of the RDRAM devices to said memory controller, and wherein said memory controller is capable of changing the frequency of said calibration cycles in response to a change in humidity.

9. The system of claim ~~1~~ 5, wherein the system memory comprises a plurality of RDRAM devices, and wherein said temperature sensor is located adjacent said RDRAM devices.

~~10.~~ 12. The system of claim ~~9~~ 1, wherein said at least one parameter includes the remaining life of said RDRAM devices.

~~11.~~ 10. The system of claim 5, wherein the system memory comprises a plurality of RDRAM devices arranged in multiple channels, and wherein at least one temperature sensor is associated with each channel.

12. The system of claim 10, further comprising a second environmental sensor associated with each channel to measure a second environmental parameter in the vicinity of each channel.

13. The system of claim 1, wherein said at least one parameter includes the error profile of said system memory.

14. The system of claim 13, wherein said system memory comprises a plurality of RDRAM memory devices, and said error profile indicates the number of memory errors that have occurred in said RDRAM memory devices.

15. The system of claim 13, wherein said system memory includes a plurality of RDRAM memory devices arranged in multiple channels, and said error profile indicates the number of memory errors that have occurred in a particular channel.

16. The system of claim 1, wherein said system memory includes one or more RDRAM devices, and said at least one parameter includes the temperature in the vicinity of the RDRAM devices.

17. The system of claim 1, wherein said system memory includes a plurality of high-speed DRAM memory devices arranged in channels, with an environmental sensor associated with each channel, and said memory controller includes control logic that modifies the frequency of said

calibration cycles in a channel in response to the environmental parameter detected by said environmental sensor associated with that channel.

18. The system of claim 17, wherein said environmental sensor comprises a temperature sensor.

19. The system of claim 17, wherein the environmental sensor comprises a humidity sensor.

20. The system of claim 1, wherein said system memory includes a plurality of high-speed DRAM memory devices, and said memory controller monitors the expected life of the DRAM memory devices, the number of memory errors occurring in the DRAM memory devices, and the temperature in the vicinity of the DRAM devices, in determining whether to change the frequency of the calibration cycles.

21. The system of claim 20, wherein the memory controller also monitors another environmental condition in the vicinity of the DRAM devices in determining whether to change the frequency of the calibration cycles.

22. The system of claim 21, wherein the environmental condition comprises humidity.

23. The system of claim 20, wherein the environmental condition comprises a light parameter.

24. A computer system, comprising:

a CPU;

a system memory comprising a plurality of high-speed DRAM memory devices coupled to said CPU;

a memory controller coupling said system memory to said CPU, said memory controller controlling and formatting transactions to the DRAM memory devices, and wherein said memory controller monitors an operating condition that may affect the operation of said DRAM memory devices; and

wherein said memory controller periodically runs calibration cycles to said DRAM memory devices, and wherein said memory controller modifies the frequency of at least one of said calibration cycles in response to a change in the operating condition.

25. The system of claim 24, wherein said high-speed DRAM memory devices comprise Direct RDRAM memory devices.

26. The system of claim 24, wherein the calibration cycles comprise a temperature calibration cycle.

27. The system of claim 24, wherein the calibration cycles comprise a current calibration cycle.

28. The system of claim 24, wherein said memory controller measures the operating condition via signals received from an environmental sensor positioned adjacent said DRAM memory devices.

29. The system of claim 28, wherein said environmental sensor includes a plurality of temperature sensors, with a separate temperature associated with each RDRAM device.

30. The system of claim 28, wherein said memory controller measures the operating condition via signals received from a second environmental sensor located adjacent said DRAM devices.

31. The system of claim 28, wherein the memory controller includes a Rambus interface module and a timer, and wherein said interface module runs calibration cycles periodically as indicated by said timer.

32. The system of claim 31, wherein the memory controller further includes control logic that receives signals from a temperature sensor, and in response, changes the value in said timer to vary the frequency of the calibration cycle.

33. The system of claim 32, wherein said memory controller further comprises an analog-to-digital converter that converts the signal from said temperature signal to a digital value for processing by said control logic.

34. The system of claim 28, wherein the system memory comprises a plurality of RDRAM devices arranged in multiple channels, and wherein at least one temperature sensor is associated with each channel.

35. The system of claim 28, wherein said operating condition includes the expected remaining life of each of said DRAM devices.

36. The computer system of claim 28, wherein said operating condition includes the number of errors occurring said DRAM memory devices.

37. A computer system, comprising:

a CPU;

a memory controller coupled to said CPU;

a video controller coupled to said memory controller;

an I/O controller hub coupled to said memory controller, said I/O controller hub connecting to at least one peripheral bus for coupling to a peripheral device;

a system memory comprised of multiple DRAM memory devices coupled to said memory controller, with said memory controller controlling and formatting transactions to the DRAM memory devices originating from said CPU and other computer system components, including said peripheral device;

wherein said memory controller runs calibration cycles to said DRAM memory devices to re-calibrate said memory devices, and wherein said memory controller is capable of varying the frequency of said calibration cycles based on an error profile of said DRAM memory devices.

38. A computer system, comprising:

a CPU;

a memory controller coupled to said CPU;

a video controller coupled to said memory controller;

an I/O controller hub coupled to said memory controller, said I/O controller hub connecting to at least one peripheral bus for coupling to a peripheral device;

a system memory comprised of multiple DRAM memory device coupled to said memory controller, with said memory controller controlling and formatting transactions to the DRAM memory devices originating from said CPU and other computer system components, including said peripheral device;

wherein said memory controller runs calibration cycles to said DRAM memory devices to re-calibrate said memory devices, and wherein said memory controller is capable of varying the frequency of said calibration cycles based on the expected remaining life of at least one of said DRAM memory devices.